AN10170

Design guidelines for COG modules with NXP monochrome LCD drivers

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Document information

Info	Content
Keywords	ITO layout, LCD driver
Abstract	This application note explains how to design the optimal ITO layout on the input side of the LCD driver IC. These design guidelines apply to all NXP monochrome LCD driver ICs unless stated otherwise. The guidelines will help toward successful first time module design and better overall display performance.

Revision history

Rev	Date	Description
03	20090608	• The format of this application note has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.
02	20030205	added section ‘Exception to the general rule’.
01	20021119	first release

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1. Introduction

In COG applications the designer must not neglect the resistance of ITO tracks. You must pay special attention to ITO layout in order to keep the effects of track resistance to an acceptable level. This Application Note explains how to design the optimal ITO layout on the input side of the driver IC for various power supply lines.

1.1 Who should read this application note?

It is important that engineers in charge of the LCD module design and ITO layout design on the interface side read this application note. Both module maker and OEM (set-maker) will find this application note useful.

2. Guidelines for power supply lines V_{SS}, V_{DD} and V_{LCD}

For COG applications the power supply circuits of NXP LCD driver ICs are separated internally into V_{DD1}, V_{DD2}, V_{DD3}, V_{SS1} and V_{SS2} supply rails. This allows the module maker to connect these supply circuits using separate ITO tracks. In this way the common (shared) part of the ITO track is minimized or eliminated. This reduces the amount of common-mode electrical noise.

For similar reasons, the LC drive supply circuits are separated internally into V_{LCDIN}, V_{LCDOUT} and $V_{LCDSENSE}$. The shared part of the ITO supply track is kept to a minimum.

Figure 1 and Figure 2 represent the ITO and glass-to-PCB connection paths in two typical configurations. Suggested maximum resistance values of the power supply for a typical small display application (pixel size approximately 0.25 x 0.25 mm^2) are given in Table 1. These limits depend on the display load and you will have to revise them for each particular application.

Excessive track resistance, especially common (shared) track and connection resistance will result in:

- a deterioration of the display quality
- increased power consumption
- incorrect operation.

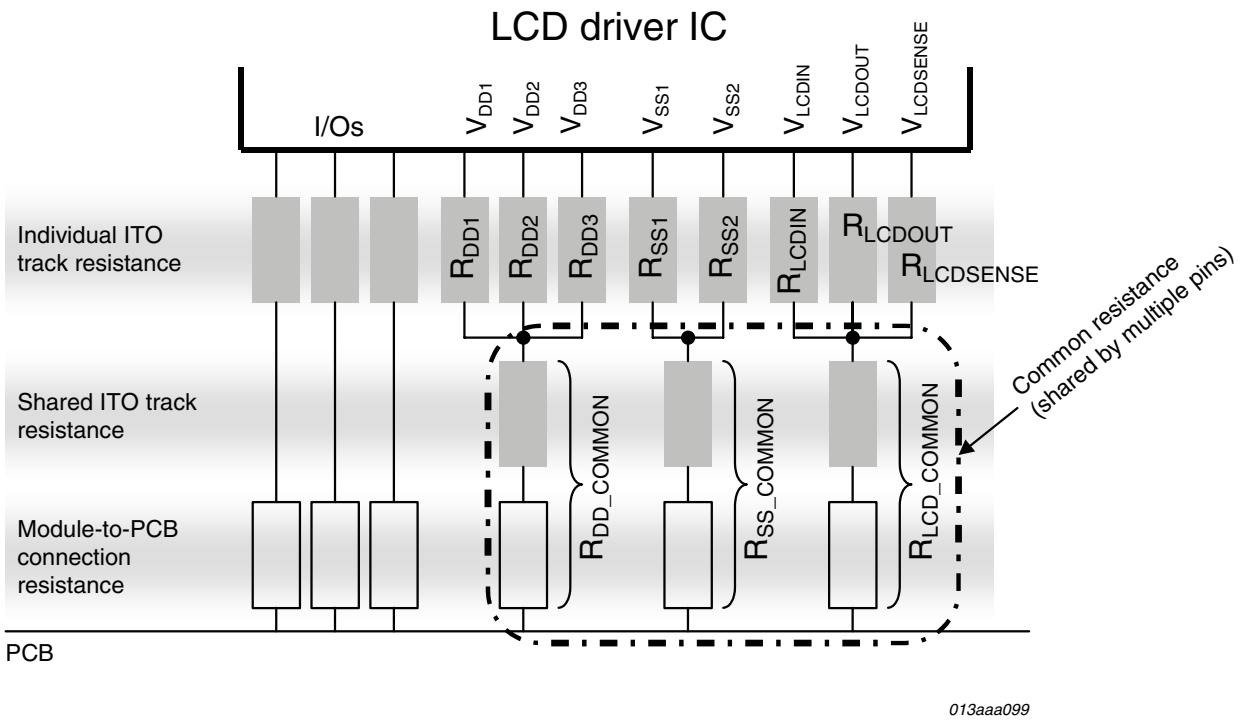

Fig 1. $V_{DD1} = V_{DD2} = V_{DD3}$

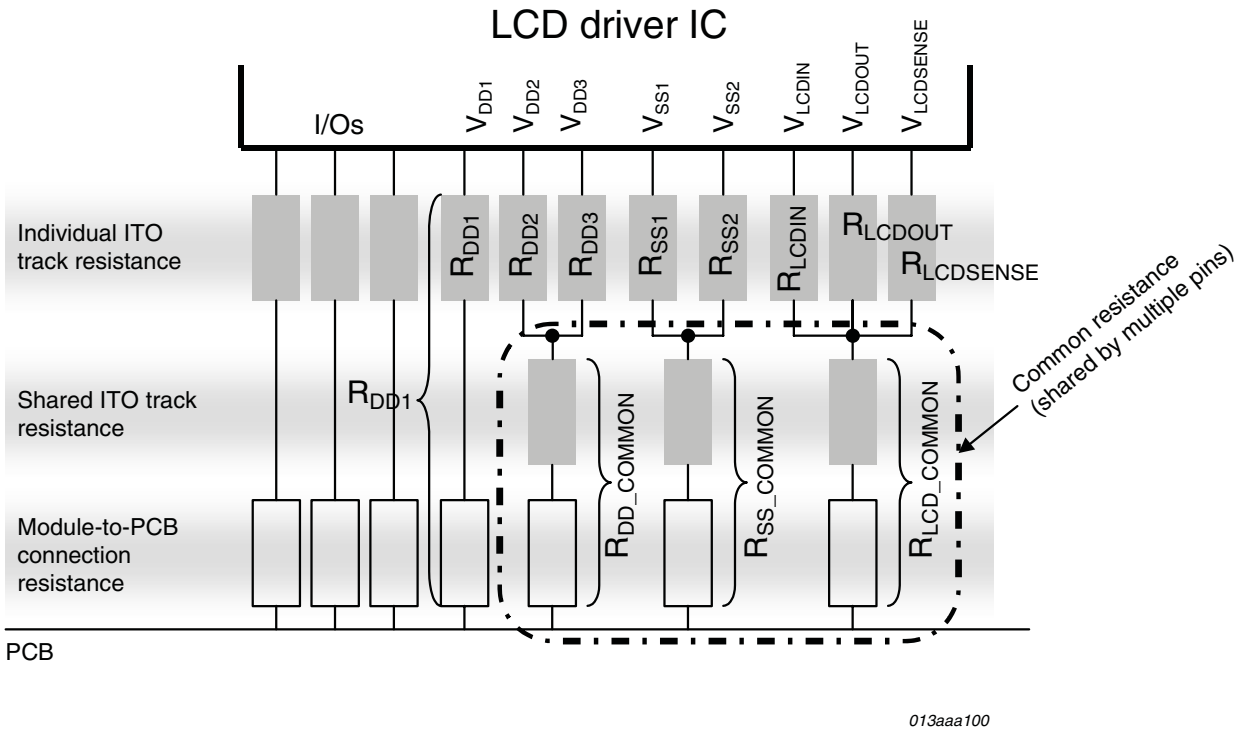

Fig 2. $V_{DD1} \neq V_{DD2} \neq V_{DD3}$

Table 1. Maximum ITO track resistance

Resistance path	Description		Maximum resistance (Ω)
R_{DD_COMMON}	common V_{DD} track (including connector)	[1]	40
R_{DD1}	positive logic supply		500
R_{DD2}	positive charge pump supply		200
R_{DD3}	positive analogue supply		2000
R_{SS_COMMON}	common V_{SS} track (including connector)	[1]	40
R_{SS1}	negative supply (excluding charge pump)		80
R_{SS2}	negative charge pump supply		200
R_{LCD_COMMON}	common V_{LCD} track (including connector)	[1]	60
R_{LCDOUT}	generated output V_{LCD}		100
R_{LCDIN}	V_{LCD} input to chip		500
$R_{LCDSENSE}$	V_{LCD} sense input		2000

[1] Common-mode resistance in supply circuits is the most critical element for optical display performance. It is most effectively minimized by connecting the separate ITO tracks outside of the LCD glass (on PCB, FPC, foil etc.) instead of at the connection point on the glass ledge. However this may not always be practical in the application.

Remark: In order to keep the ITO track resistance to a minimum, you must select the pitch and position of the module connection to the outside such that the power tracks run as straight as possible to the glass edge. In order to minimize common connection resistance use low-ohmic elastomeric connection, metal pin connection or ACF bonded flat cable.

Figure 3 shows an example of how the ITO layout for the power supply tracks looks in practice.

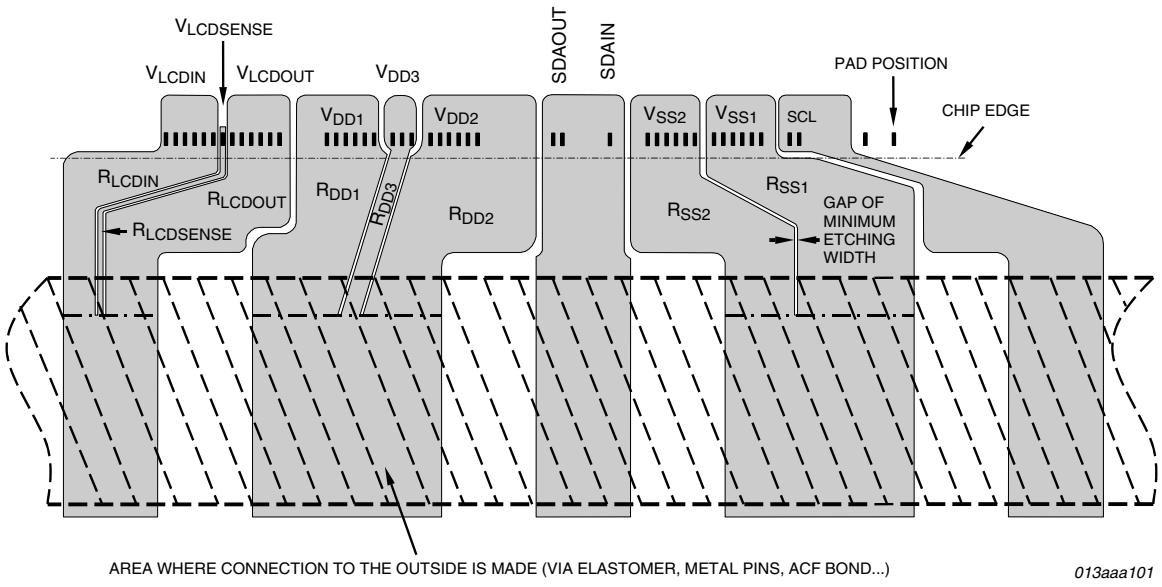

Fig 3. ITO layout example for V_{SS}, V_{DD} and V_{LCD}

2.1 Exception to the general rule

The PCF8811 LCD driver uses a slightly different power architecture where the V_{LCD} voltage generation is concerned. Because of this, the ITO layout guidelines for connecting pins V_{LCDIN}, V_{LCDOUT}, $V_{LCDSENSE}$ are also different (see Table 2).

Table 2. Exception

Resistance path	Description	Maximum resistance (Ω)
R_{LCD_COMMON}	common V_{LCD} track (including connector)	60
R_{LCDOUT}	generated output V_{LCD}	0
R_{LCDIN}	V_{LCD} input to chip	0
$R_{LCDSENSE}$	V_{LCD} sense input	0

In practice this means that you must connect V_{LCDIN}, V_{LCDOUT} and $V_{LCDSENSE}$ together with one thick ITO track.

3. Guidelines for I/O lines

ITO track impedance also affects the AC characteristics of the I/O lines. The ITO track resistance together with any parasitic capacitances adds RC-type delay constants which you must take into account. NXP recommends that COG modules are not operated close to the limits of the interface timing requirements. You must also pay particular attention to open-drain outputs (see Section 4).

4. Guidelines for I²C-bus pins SDA and SCL

The SDA line in I²C devices is an open-drain output and therefore needs an external pull-up resistor. The ITO track resistance, R_{ITO}, together with the pull-up resistor, $R_{PULL-UP}$, forms a potential divider. Because of this there is a danger that the other device(s) on the I²C-bus will not see a valid logic LOW when the LCD driver IC drives the SDA line LOW e.g. during the ACKnowledge cycle or during read-back from the IC (see Figure 4).

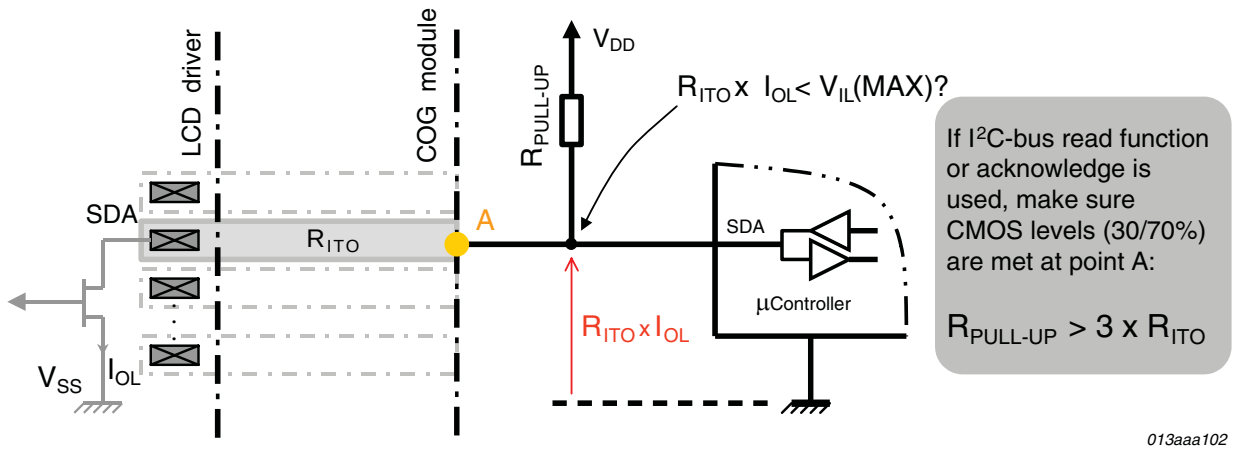

Fig 4. Effects of the ITO resistance in the SDA line

For this reason the SDA signal in LCD driver ICs is sometimes split into SDAIN and SDAOUT. A number of possibilities for connecting LCD to the host micro exist, three examples are given.

- The I²C protocol is fully implemented in the system, i.e. the master-transmitter device (host microcontroller) expects an ACKnowledge after each byte. In this case connect LCD driver's SDAIN and SDAOUT pins on glass with a single ITO trace, taking care to minimize track and connection resistance. Choose a pull-up resistor value that will ensure that the V_{IL} spec of the other device(s) on the I²C-bus is always met, under all conditions and including all tolerances. Note that the value of $R_{PULL-UP}$ directly affects the SDA signal rise time. Take care that $R_{PULL-UP}$ is not too high that the maximum rise time limit is violated. A simple rule in this case is to make sure that $(2 \times C_{SDA} \times R_{PULL-UP}) < t_R(max)$, where C_{SDA} is the capacitance of the SDA bus rail, including the associated parasitic pad capacitances of all the devices connected to the I²C-bus and $t_R(max)$ is the specified maximum rise time (see Figure 5).

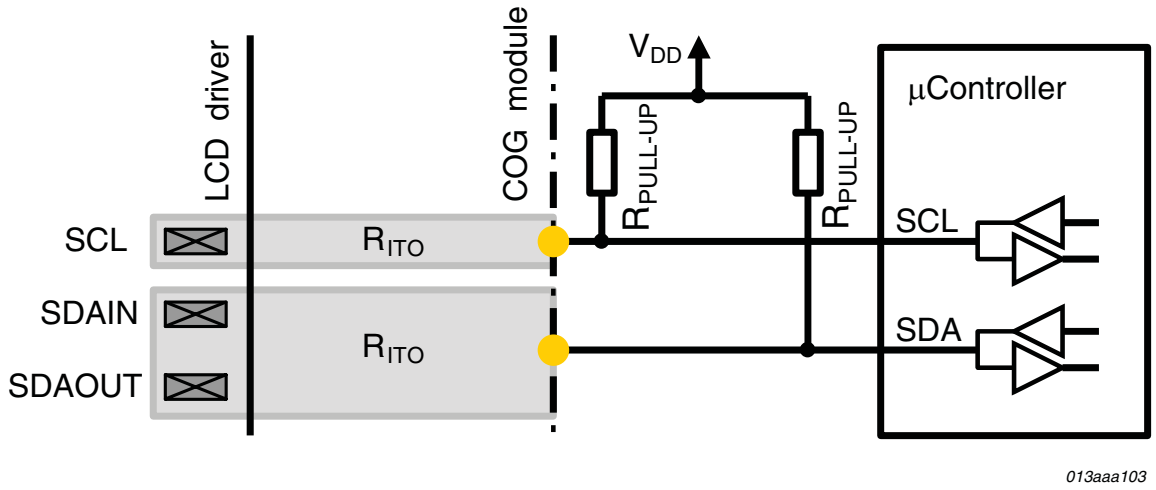

Fig 5. Typical configuration: direct connection to the microcontroller

- The I²C protocol is fully implemented in the system but the value of the pull-up resistor required to satisfy the *maximum logic low level* requirement $V_{IL}(max)$ is too high to satisfy simultaneously the *maximum rise time* requirement, t_R. In this case the full SDA signal may be reconstituted using an external open-drain buffer (see Figure 6). The buffer isolates the SDAOUT pin from the capacitance of the I²C-bus and makes the rise time requirement easier to meet.

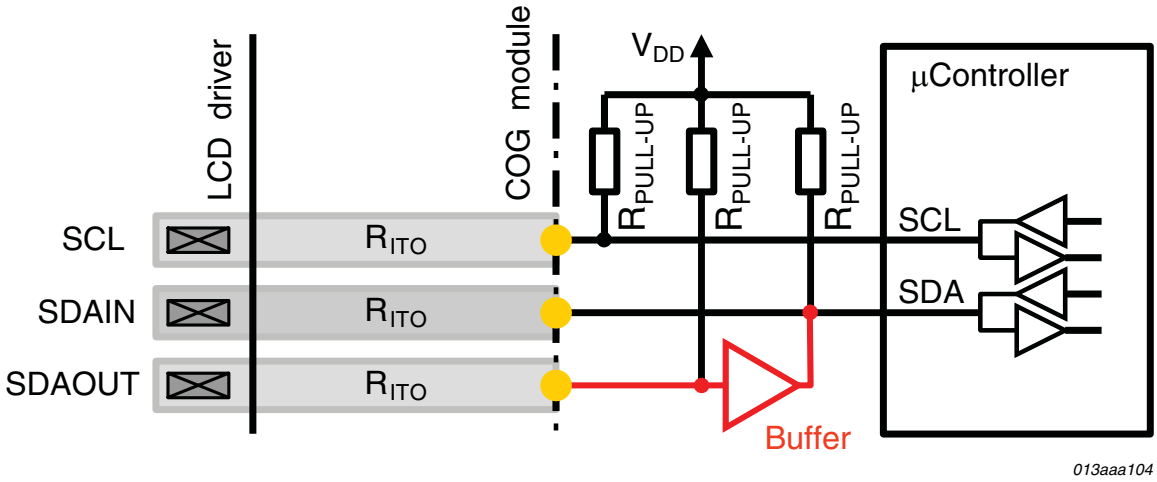

Fig 6. Connection to a microcontroller using an open-drain buffer

- It is possible to implement the I²C protocol partially, in a way that ignores the ACKnowledge bit after each byte. In this case you can leave the SDAOUT unconnected (see Figure 7). Such a configuration may be desirable because it eliminates the common-mode noise that results from the ACKnowledge current flowing through the common resistance in the V_{SS} supply of the driver IC. Note however that in this case it is not possible to use any read-back function which is implemented in the LCD driver IC.

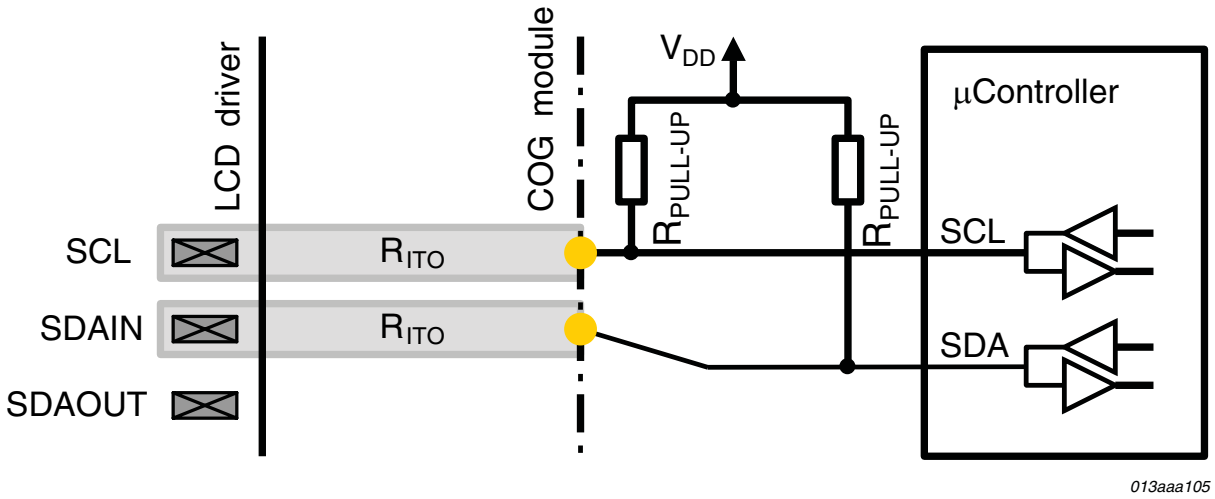

Fig 7. No connection to SDAOUT pin

5. Guidelines for ESD/EMC protection

5.1 Dummy pads

You must not connect dummy pads (test or reserve pads) to ITO tracks. Connecting dummy pads may compromise the ESD protection of the LCD module because these pads have no ESD protection elements.

5.2 Hardware reset pad

In COG applications the interface and supply lines have a higher impedance compared to COB, TCP, or COF. The resistance of individual lines may differ in value considerably from one ITO track to the next. This difference may be hundreds of ohms. As a result it is possible to generate a large differential voltage across the ITO tracks during an EMC event. The RESET pad recognizes such an EMI-induced voltage spike (of the order of 5 ns) as a reset command. To prevent this a low-pass filter is built into the RESET pad of the LCD driver ICs.

The PCF8531/F1 requires an external ITO resistor to be placed directly underneath the IC die in order to create a first order low-pass filter together with the parasitic pad capacitance (see Figure 8).

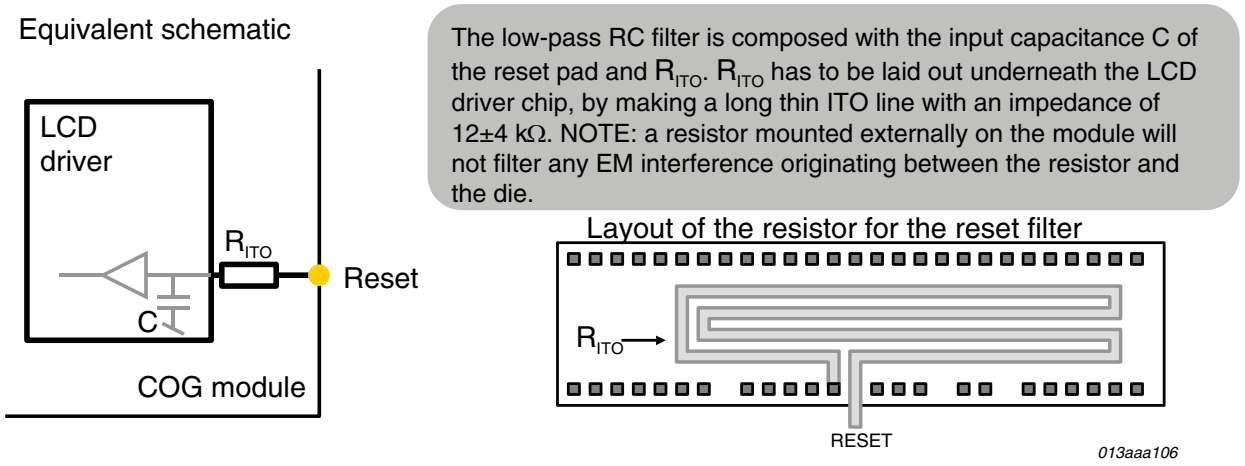

Fig 8. ITO meander resistor for EMC low-pass filter

5.3 Power supply tracks V_{SS} and V_{DD}

To further increase EMC immunity NXP recommends that you reduce as much as possible the resistance of the ITO tracks and connections for the power supply - V_{DD1}, V_{DD2}, V_{DD3}, V_{SS1}, V_{SS2}.

5.4 Unused pins

When pins are not used in the application (e.g. test pins, unused interface pins etc.) it may be a requirement that these pins are tied to V_{DD1} or V_{SS1} (*tied off*). In this case it is important to make the connection to V_{DD1} or V_{SS1} as direct as possible. Sometimes so-called *tie-off* pads are provided for this purpose (called Vxx1 TIEOFF or similar). If there are no tie-off pads then you must make the connection directly to the V_{DD1} or V_{SS1} pads (see Figure 9).

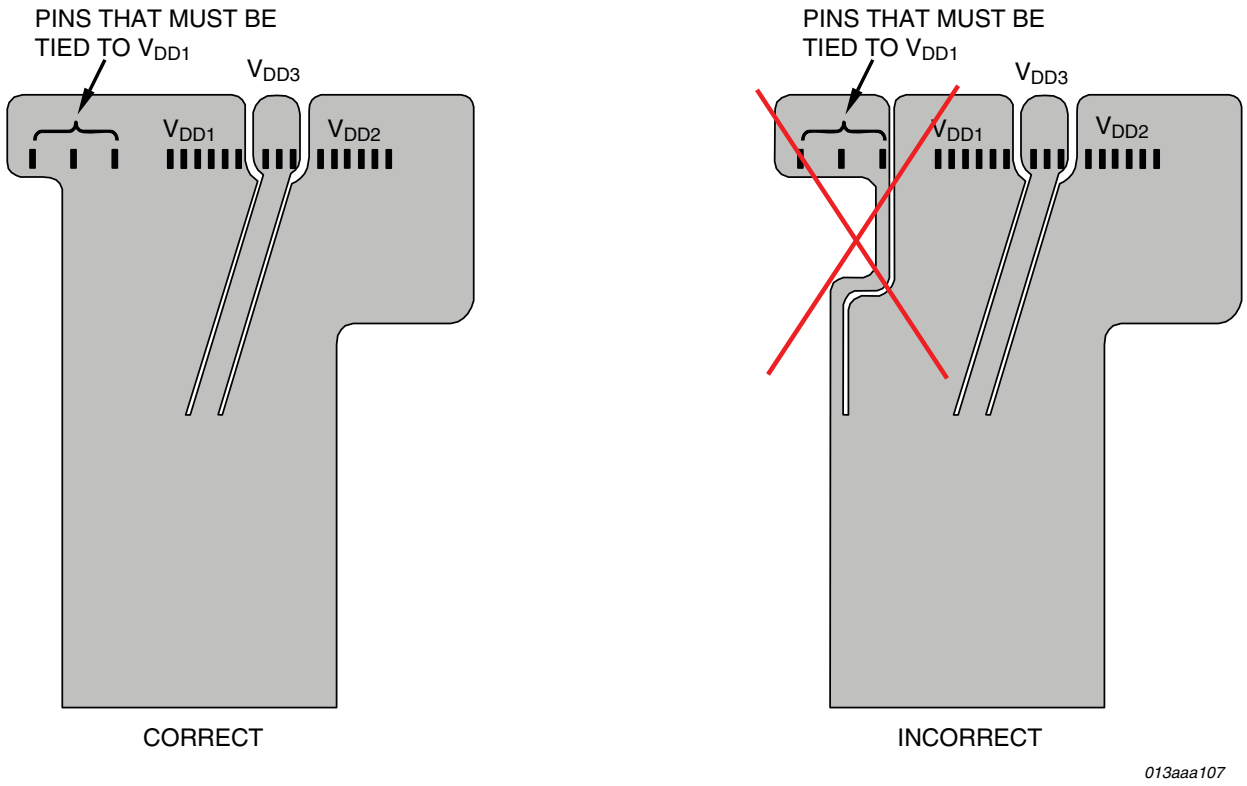

Fig 9. Tie off for unused pins

6. Guidelines for COG mounting

6.1 COG bonding conditions

The COG bonding conditions described are based on practical experience within NXP Semiconductors and must be used as a guideline. The COG bonding conditions in each application must be validated using reliability and reproducibility tests. Special care must be taken in analyzing the following parameters after COG bonding to prevent abnormalities:

- bump height
- bump deformation
- bump roughness
- IC passivation integrity
- uniform ACF particle density.

Special care must be taken in the COG bonding production facility to:

- avoid dust and other alien particles to interfering with the COG bonding process
- avoid ESD overstress during COG bonding.

6.2 COG Bonding parameters

Figure 10 shows a drawing of COG bonding with ACF.

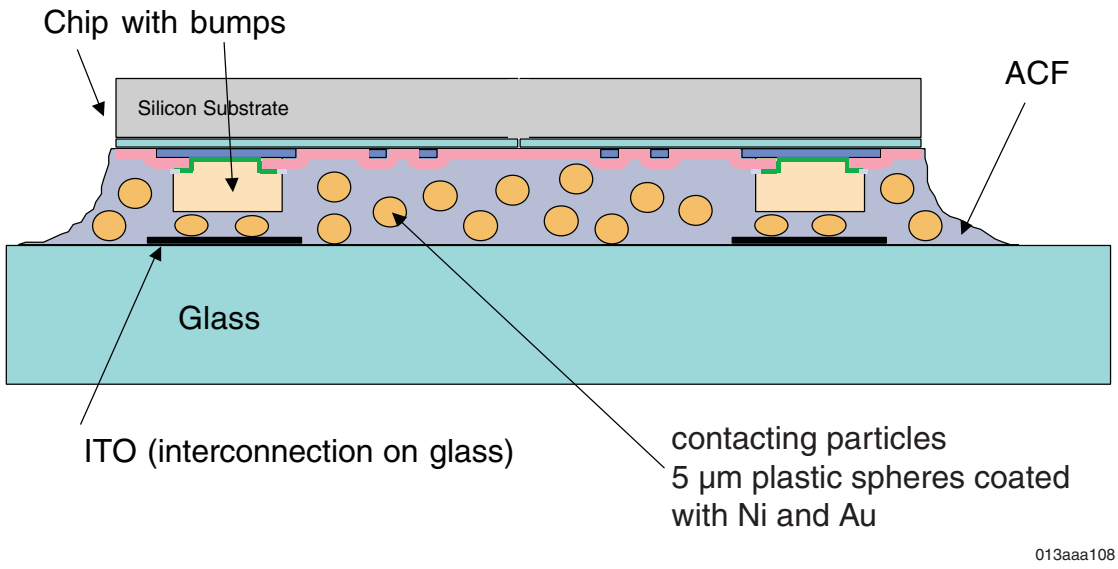

Fig 10. COG bonding

The following parameters apply to all COG bonding (Au bumps) processes:

- bonding pressure as a function of total bump area of the IC: 12 kg / mm^2
- ACF temperature 220 °C ± 10 °C.

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